CLAIMS

1. A method of testing the integrity of a plurality of semiconductor device connections within a product containing one or more semiconductor devices, wherein one or more semiconductor devices include a non-linear element in a conduction path between a first node and a second node connected to a power supply connection of the devices; the method comprising the steps of:

applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes,

making measurements of the voltage difference as the test current varies, and

on the basis of the measurements extracting a response component due predominantly to the non-linear characteristic of the devices and using this to indicate whether said semiconductor device connections are acceptable.

2. A method as claimed in claim 1, in which measured voltage difference values and their respective test current values are analysed to calculate an offset voltage for the dynamic resistance of the circuit.

3. A method as claimed in claim 2, wherein the non-linear devices are diodes and the offset voltage is a function of the number of diodes passing the current between the first and second nodes.

4. A method as claimed in any preceding claim in which the test signal is supplied from a current source.

5. A method as claimed in claim 1, in which the test signal comprises a DC signal of switchable value.

6. A method as claimed in claim 1, in which the test signal comprises an AC signal.

7. A method as claimed in claim 6, in which harmonics of the AC signal generated by virtue of current flow in the non-linear devices are detected in order to indicate the presence of the non-linear devices.

8. A method as claimed in claim 7, in which the magnitude of a harmonic component is used as a measure of the number of non-linear devices connected between the first and second nodes.

9. A method as claimed in claim 1 in which the test signal comprises discrete time samples of a sinusoidal or other waveform having little or zero low-order harmonic content, and the measured voltage differences are used as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero low-order harmonic content input for harmonic analysis.

10. A method of testing the continuity of a connection between an integrated circuit pin and a circuit board where the integrated circuit pin is connected to a plurality of integrated circuit pins forming a first group, the method comprising the steps of:

identifying a second group of integrated circuit pins having electrical properties relatable to the first group;

applying one or more first test signals to the first group of pins and measuring one or more respective first voltage differences occurring between the first group of pins and a reference voltage;

applying one or more second test signals to the second group of pins and measuring one or more respective second voltage differences occurring between the second group of pins and a reference voltage; and

on the basis of measurements extracting and comparing a non-linear characteristic of the first and second group of pins to obtain a measure of said continuity.

11. A method as claimed in claim 10, in which the first and second groups comprise the same number of device pins.

12. A method as claimed in claim 11, in which each device connection in the first group has a corresponding device connection in the second group being members of the same or similar family of device technologies and of similar function.

13. A method as claimed in claim 10, in which the first and second non-linear characteristics are compared and a faulty connection is indicated if the difference between them exceeds a first threshold.

14. A method as claimed in claim 10, in which the first test signals and the second test signals are substantially identical current waveforms.

15. A method as claimed in claim 10, in which the first test signals and the second test signals are DC signals of switchable value and voltage offsets are calculated from the voltage differences, the offsets are compared and a faulty connection is indicated if the difference in offsets exceeds a threshold value.

16. A method as claimed in claim 10, in which the or each first test signal and the or each second test signal comprises an AC component superimposed on a DC component and the magnitude of harmonic components are compared and a faulty connection is indicated if the difference in harmonic components exceeds a threshold value.

17. A method as claimed in claim 10, in which the or each first test signal and the or each second test signal comprises discrete time samples of a sinusoidal or other waveform having little or zero low-order harmonic content, and the measured voltage differences are used as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero low-order harmonic content input for harmonic analysis.

18. A method as claimed in claim 10, in which the comparison of non-linear characteristics is performed directly by extracting a non-linear characteristic based on forming a difference between the first voltage difference and the second voltage difference.

19. An apparatus for testing the integrity of a plurality of device connections within a product containing one or more devices, wherein one or more devices include a non-linear element in a conduction path between a first node and a second node connected to a power supply connection of each device, the apparatus comprising:

signal means for applying a test signal to the devices such that a test current flows between said nodes creating a voltage difference between said nodes,

a voltage measuring device for making measurements of the voltage difference as the test current varies, and

a data processor arranged on the basis of the measurements to extract a response component due predominantly to the non-linear characteristic of the devices and to use this to indicate whether said device connections are acceptable.

20. An apparatus as claimed in claim 19, in which measured voltage difference values and their respective test current values are analysed to calculate an offset voltage for the dynamic resistance of the circuit.

21. An apparatus as claimed in claim 20, wherein the non-linear devices are diodes and the offset voltage is a function of the number of diodes passing the current between the first and second nodes.

22. An apparatus as claimed in claim 19, 20 or 21, in which the test signal is supplied from a current source.

23. An apparatus as claimed in claim 19, in which the test signal comprises a DC signal of switchable value.

24. An apparatus as claimed in claim 19, in which the test signal comprises an AC signal.

25. An apparatus as claimed in claim 24, in which the harmonic components of the signal generated by virtue of current flow in at least one non-linear device are detected in order to indicate the presence of at least one non-linear device.

26. An apparatus as claimed in claim 25, in which the magnitude of a harmonic component is used as a measure of the number of non-linear devices connected between the first and second nodes.

27. An apparatus as claimed in claim 19, in which the test signal comprises discrete time samples of a sinusoidal or other waveform having little or zero low-order harmonic content, and the measured voltage differences are used as discrete samples in reconstructing the response to a sinusoidal or other waveform having little or zero low-order harmonic content input for harmonic analysis.

28. An apparatus for testing the continuity of connections in a circuit path within a product, said path comprising a plurality of integrated circuit device pins forming a first group connected to a first circuit node such that current flows via the pins and through associated semiconductor junctions to a second circuit node, the apparatus comprising:

first signal means for applying M test signals to the first group of pins and measuring M voltage differences occurring between the first circuit node and a reference, where M is an integer greater than zero;

second signal means for applying N test signals to a second group of pins expected to have a behaviour identical to or relatable to the first group of pins and measuring N voltage differences occurring between a second circuit node connected to the second group of pins and a reference, where N is an integer greater than zero; and

a processor responsive to the voltage differences for deriving or comparing a non-linear characteristic of the first and second groups of pins to obtain a measure of said continuity.

29. An apparatus as claimed in claim 28, in which the first and second groups comprise the same number of device pins.

30. An apparatus as claimed in claim 29, in which each device connection in the first group has a corresponding device connection in the second group being members of the same or similar family of device technologies and of similar function.

31. An apparatus as claimed in claim 29, in which the first and second non-linear characteristics are compared and a faulty connection is indicated by the data processor if the difference between them exceeds a first threshold.

32. An apparatus as claimed in claim 29, in which the M test signals and the N test signals are substantially identical current waveforms.

33. Apparatus as claimed in claim 28, in which the first test signals and the second test signals are DC signals of switchable value and voltage offsets are calculated from the voltage differences, the offsets are compared and a faulty connection is indicated if the difference in offsets exceeds a threshold value.

34. An apparatus as claimed in claim 29, in which the M test signals and the N test signals comprise an AC component superimposed on a DC component and the magnitude of harmonic components of the voltage differences are compared and a faulty connection is indicated if the difference in harmonic components exceeds a threshold value.

35. An apparatus as claimed in claim 28, in which the comparison of non-linear characteristics is performed directly by extracting a non-linear characteristic based on forming a difference between the first voltage difference and the second voltage difference.

36. An apparatus as claimed in claim 19 or claim 28, further comprising a further test signal generator for generating a probe current which is injected via a further device connection into a selected integrated circuit, and wherein the continuity test is

repeated and the selected integrated circuit is indicated as having an unacceptable connection if the non-linear characteristic varies by more than a first predetermined threshold, or is indicated as having an acceptable connection if the non-linear characteristic varies by more than a second predetermined threshold of opposite sign to the first predetermined threshold.

37. A method as claimed in claim 1 or claim 10, wherein a further test signal generator generates a probe current which is injected via a further device connection into a selected integrated circuit, and wherein the continuity test is repeated and the selected integrated circuit is indicated as having an unacceptable connection if the non-linear characteristic varies by more than a first predetermined threshold, or is indicated as having an acceptable connection if the non-linear characteristic varies by more than a second predetermined threshold of opposite sign to the first predetermined threshold.